Power Matters

Advantages of Microsemi SiC MOSFETs

Outline

- ❑ Technology development
- ❑ Benchmark of SiC MOSFET by Microsemi against competitors
  - DC characteristics key to switching performance
  - Dynamic performance
  - Ruggedness
- ❑ Reliable technology platform

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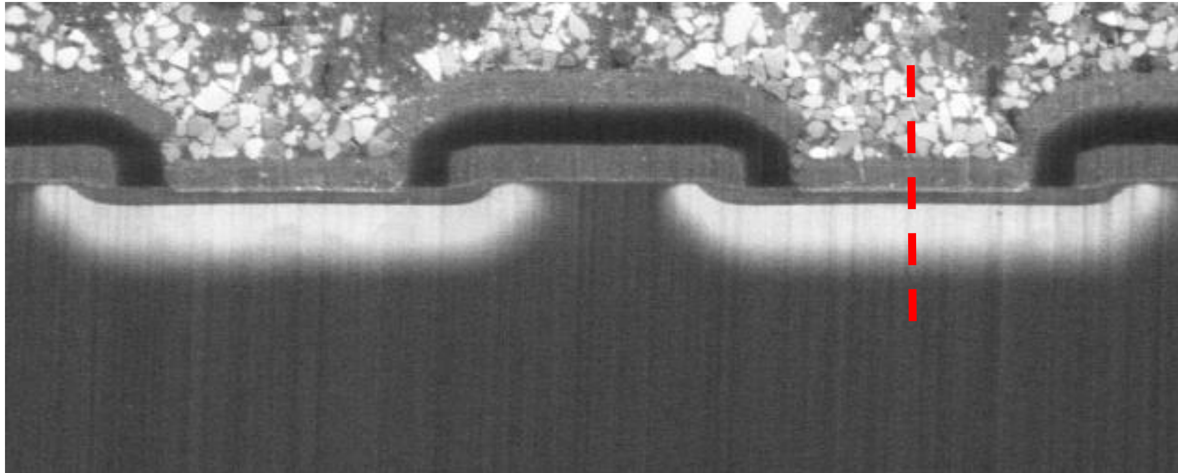
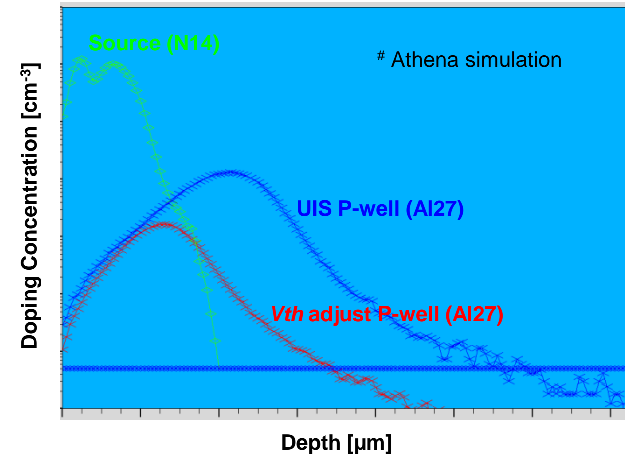
Technology Development

SiC MOSFET Transistor X-Section





- Simulation-based technology development to cut cycles of learning
- Flexibility of design variations for special applications
- Thick Al-Cu metallization for interconnect and bond pads
- 2-layer metal process integration for maximized packing density
- Thick final passivation for maximum reliability

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Contrast to Silicon Tecnology

- Dopant introduction by implant at elevated temperatures
- Dopant activation, implant damage anneal at high temperatures
- High temperature gate oxidation
- Above translates into all layer removal post dopant introduction for electrical activation
- Alignment is critical

E220
Production Implanter

CentroTherm CHV-100
Post Implant Annealing to 1700 °C

Hi Temp Oxidation
SiC MOSFET Gate Oxidation

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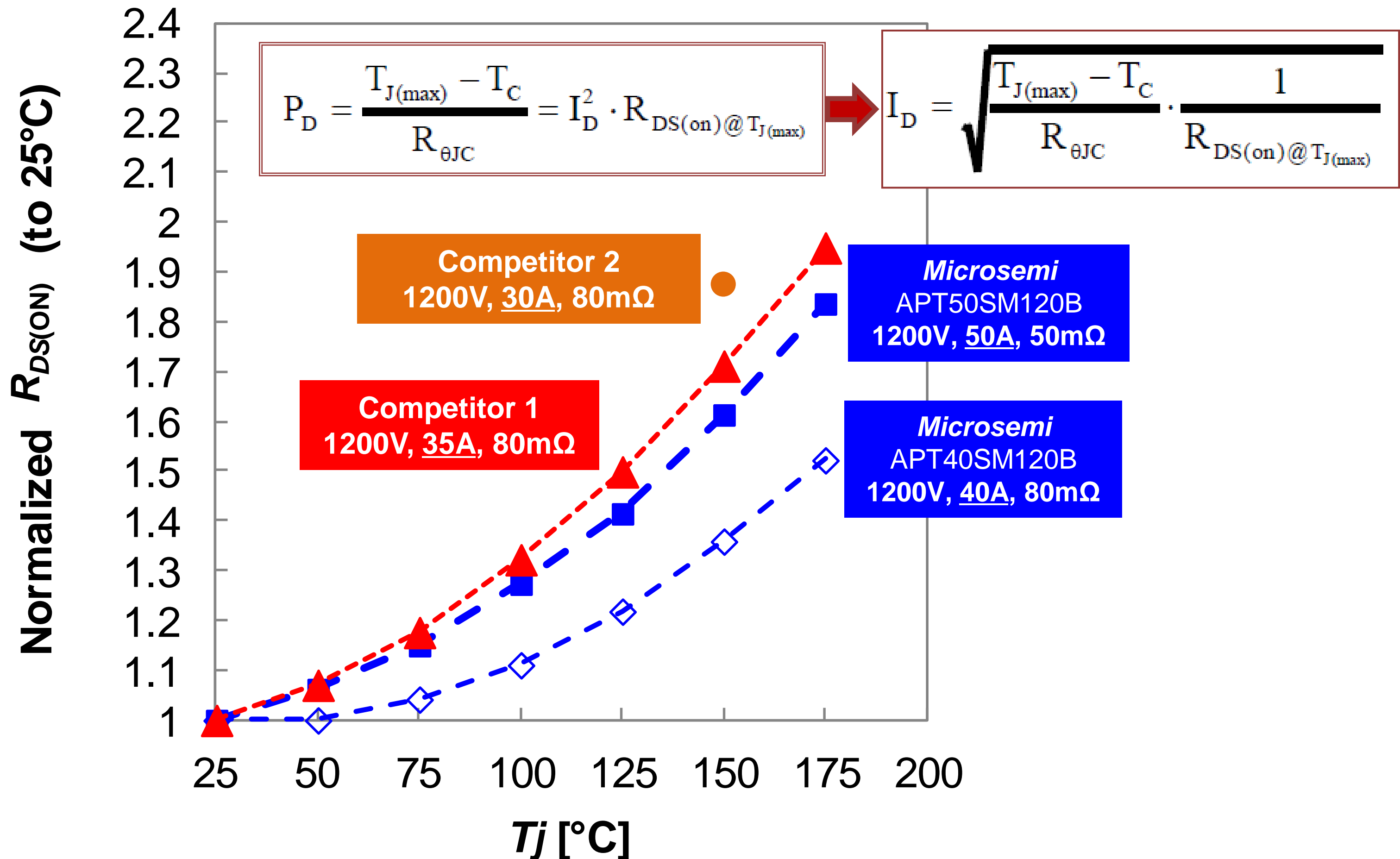
DC Characteristics Key to Switching Performance

Best in Class $R_{DS(ON)}$ vs. Temperature



- Lower $R_{DS(ON)}$ at temperature provides higher ceiling for continuous current rating

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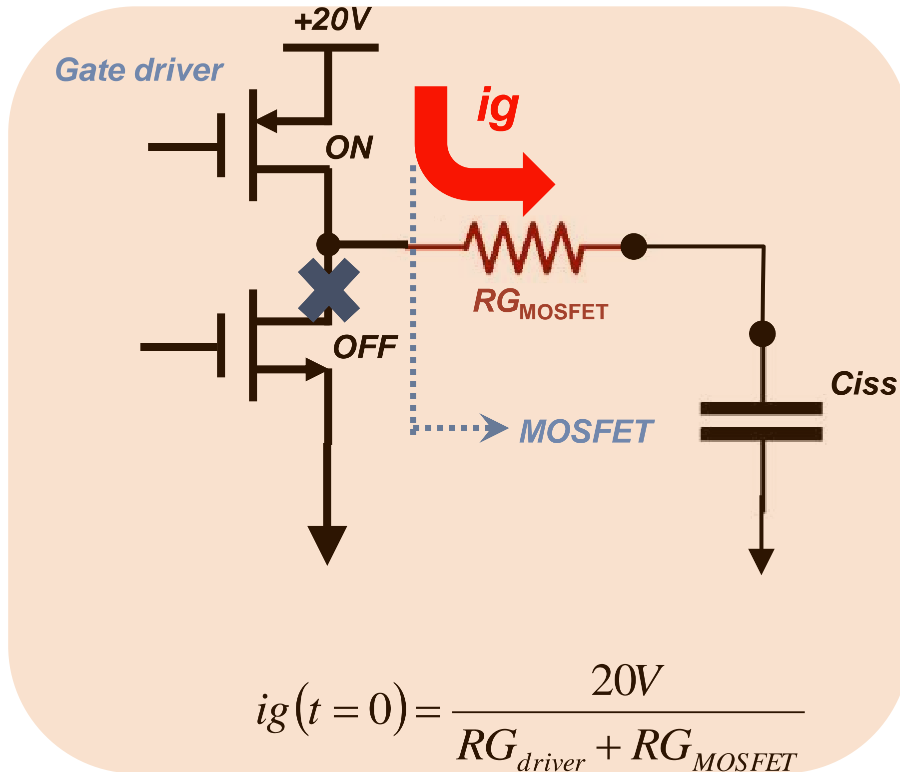
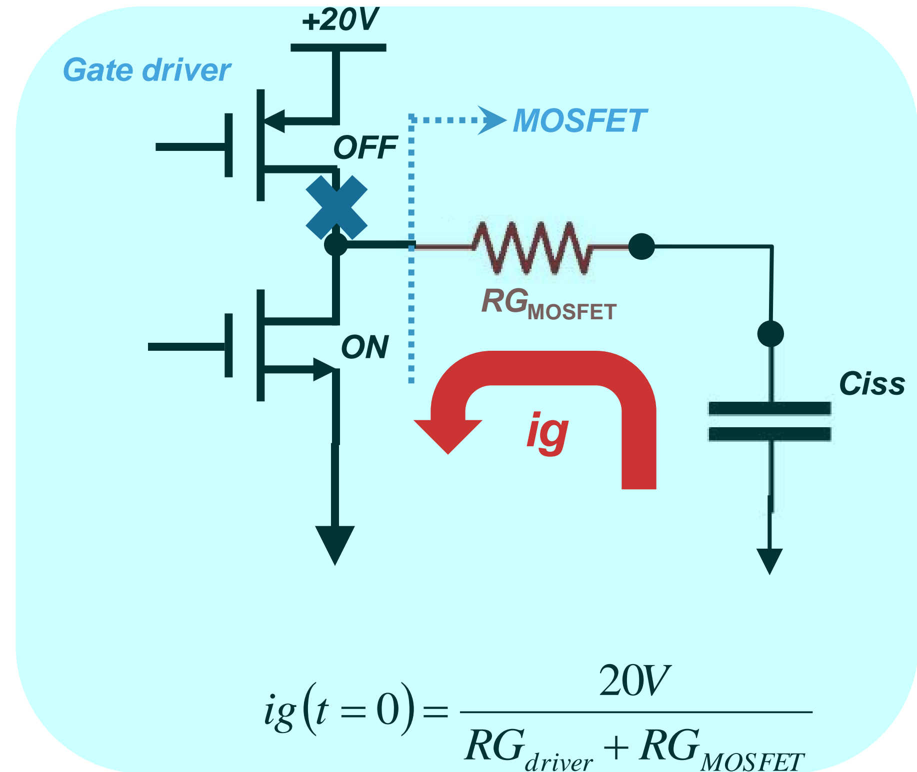
RG & Dynamic Performance

Turn-On



$$ig(t=0)=\frac{20V}{RG_{driver}+RG_{MOSFET}}$$

Turn-Off



$$ig(t=0)=\frac{20V}{RG_{driver}+RG_{MOSFET}}$$

- High gate resistance limits available charging current, consequently, retards transistor switching performance

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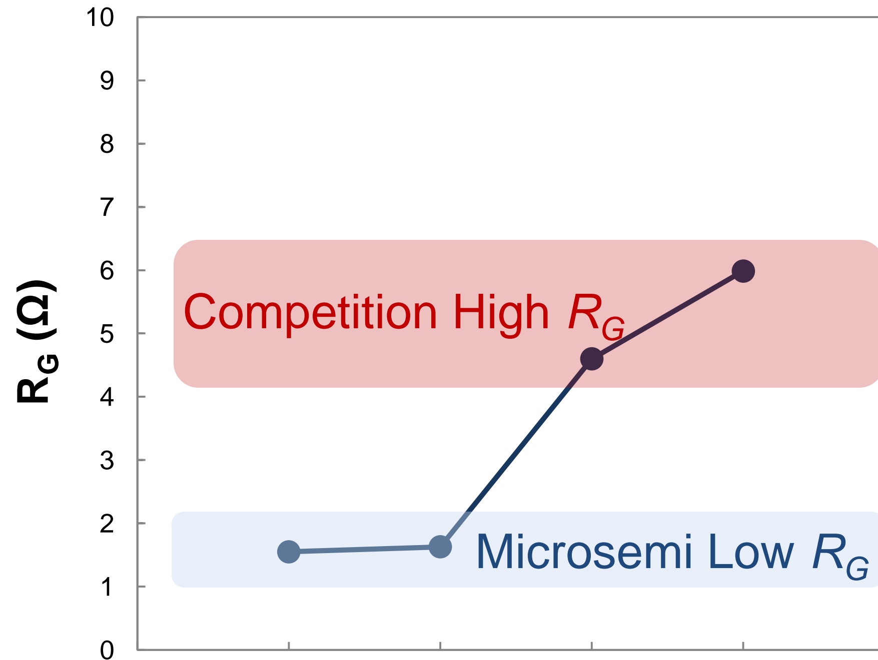
Ultra Low Gate Resistance

Minimized Switching Energy Loss & Higher Switching Frequency



Oscillation-free with minimal external R_G

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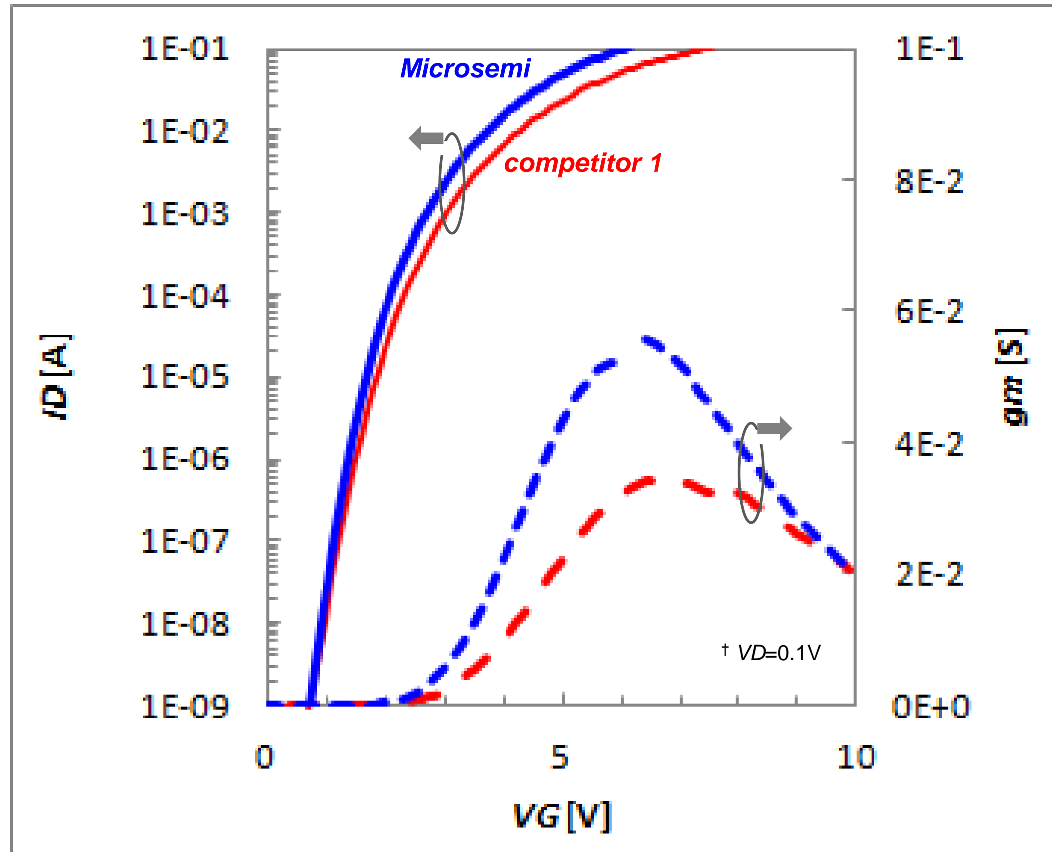
High Transconductance (*gm*) Cuts t_{ON}



- 2× *gm* at the start of the turn-on process
- Equivalent high-current *gm* (>1A)

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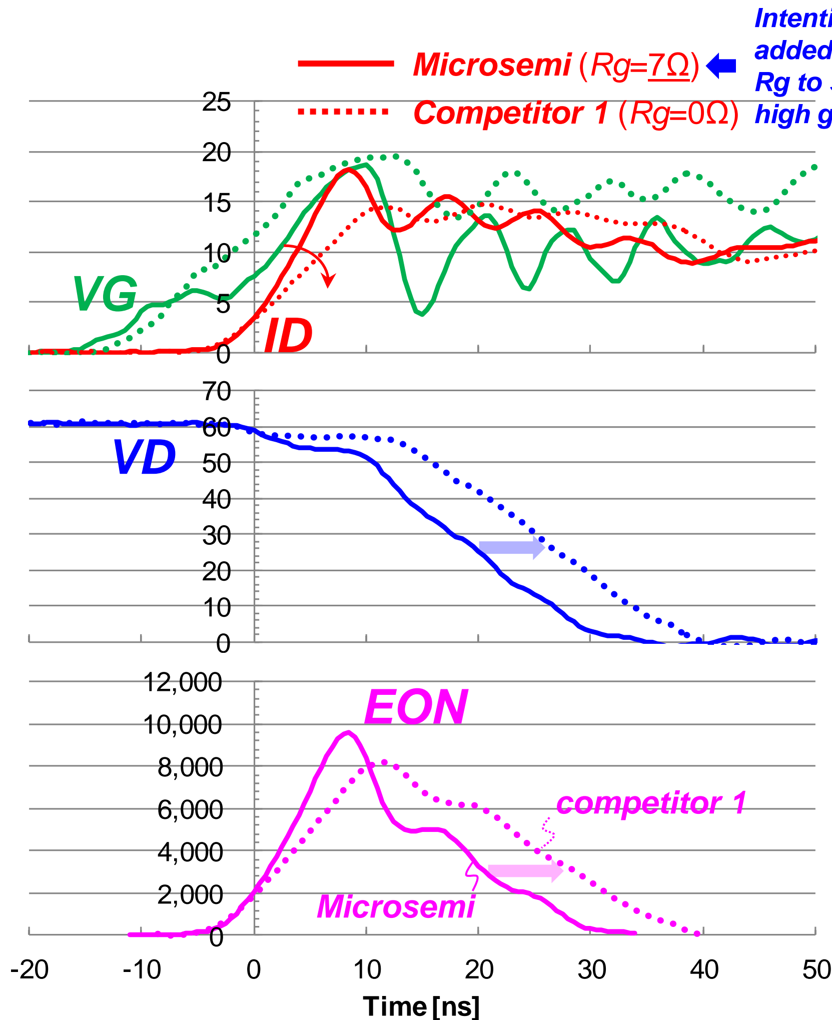
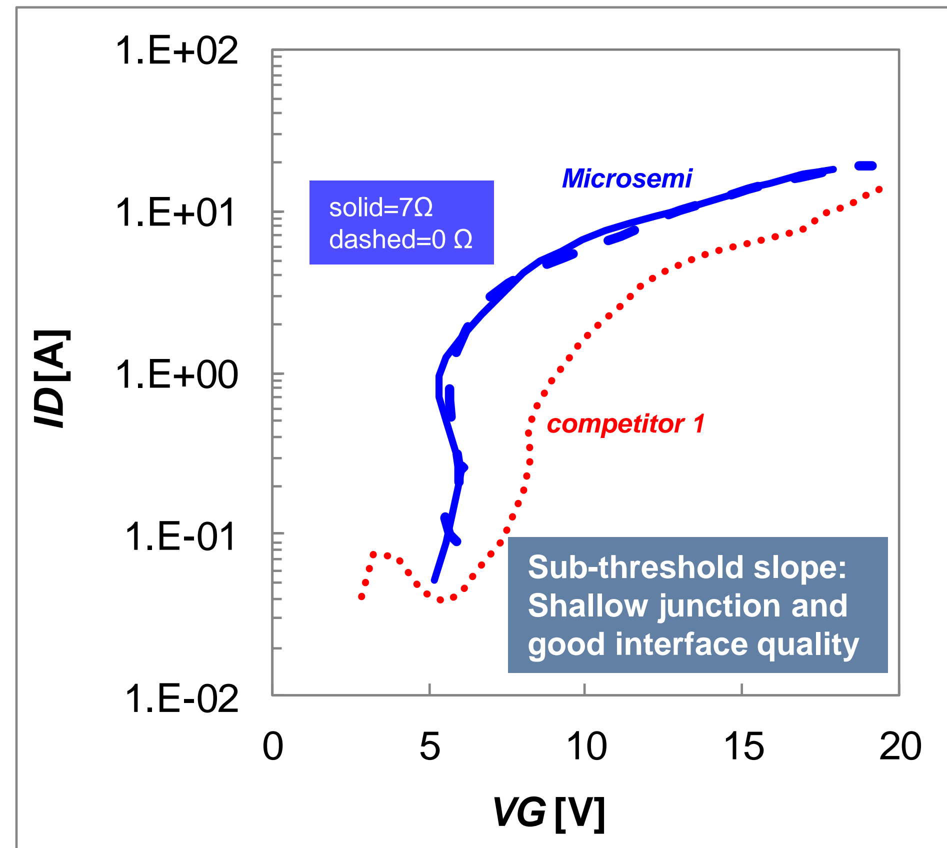
High Transconductance (*gm*) Cuts t_{ON}





- Superior sub-1A *gm* jumps start the turn-on process

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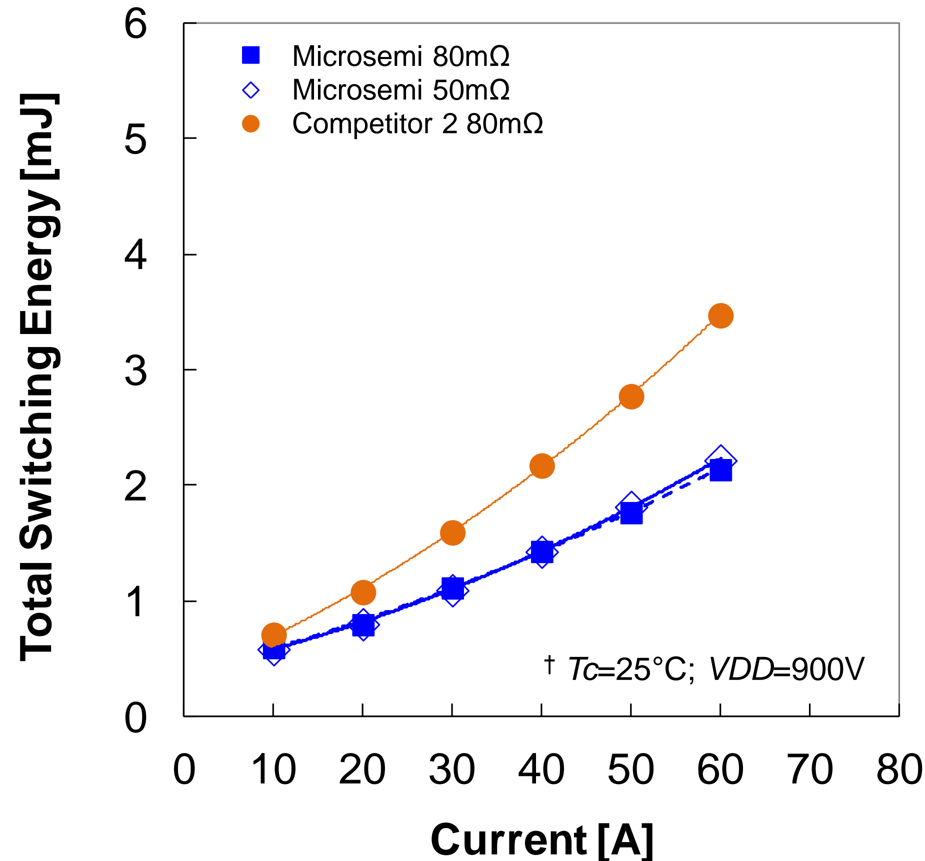
Superior Dynamic Performance

Switching Energy Benchmark



- >30% less switching loss translates to cooler dynamic operations and capability for higher switching frequencies

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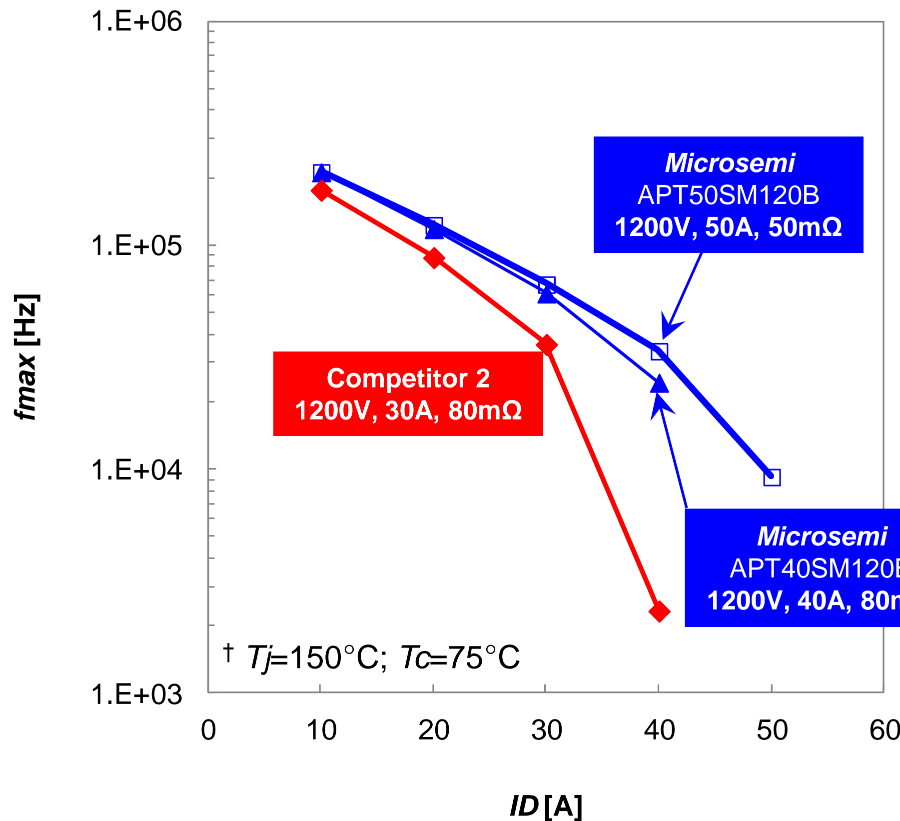
Maximum Switching Frequency, *fmax*



Limitation 1

Total switching time ≤ 5% switching period

$$f_{max1} = \frac{1}{T_s} = \frac{0.05}{t_{d(on)} + t_{d(off)} + t_r + t_f}$$

Limitation 2

Thermally limited switching frequency

$$f_{max2} = \frac{1}{t_{diss}} = \frac{\frac{T_J - T_C}{R_{\theta JC}} - P_{cond}}{E_{on2} + E_{off}}$$

$$P_{diss} = \frac{T_J - T_C}{R_{\theta JC}} = P_{cond} + \frac{E_{on2} + E_{off}}{t_{diss}}$$

Dynamic performance breakaway enablers:

- Superior ***EON*** (t_{on}) due to high ***gm***, ultra low ***RG***
- Superior ***EOFF*** due to extremely low ***RG*** (yet oscillation free with very low external ***RG***)
- Low $R_{DS(ON)}$ at high temperatures extends switching frequency and current capability

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Outstanding Ruggedness

Superior Short Circuit Withstand

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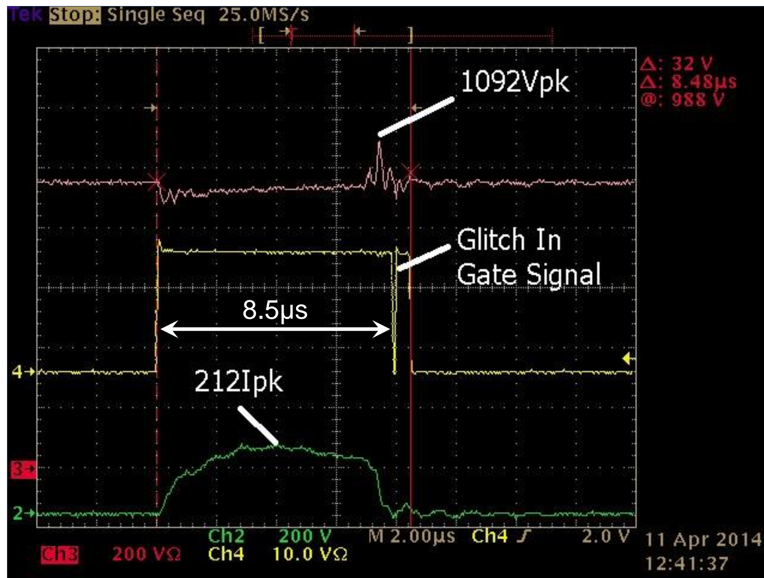
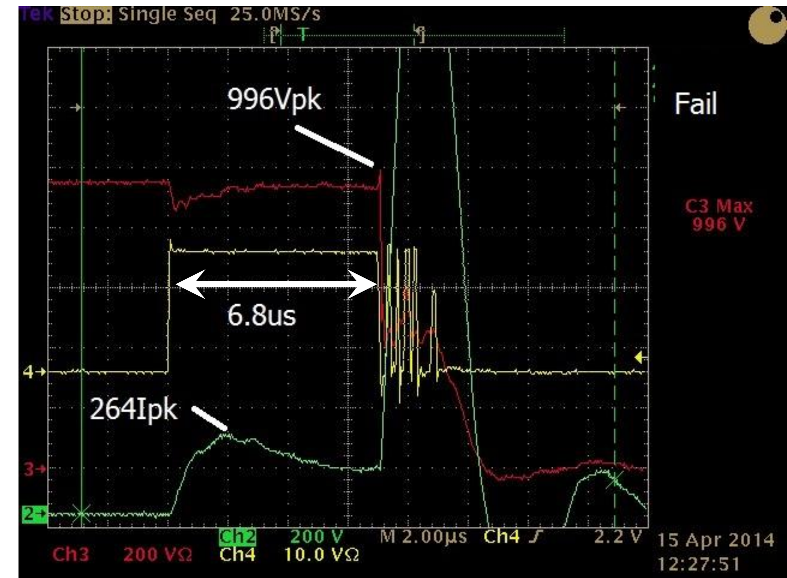


Competitor 1



- Microsemi’s 80mΩ SiC MOSFET demonstrates **25%** longer short circuit capability

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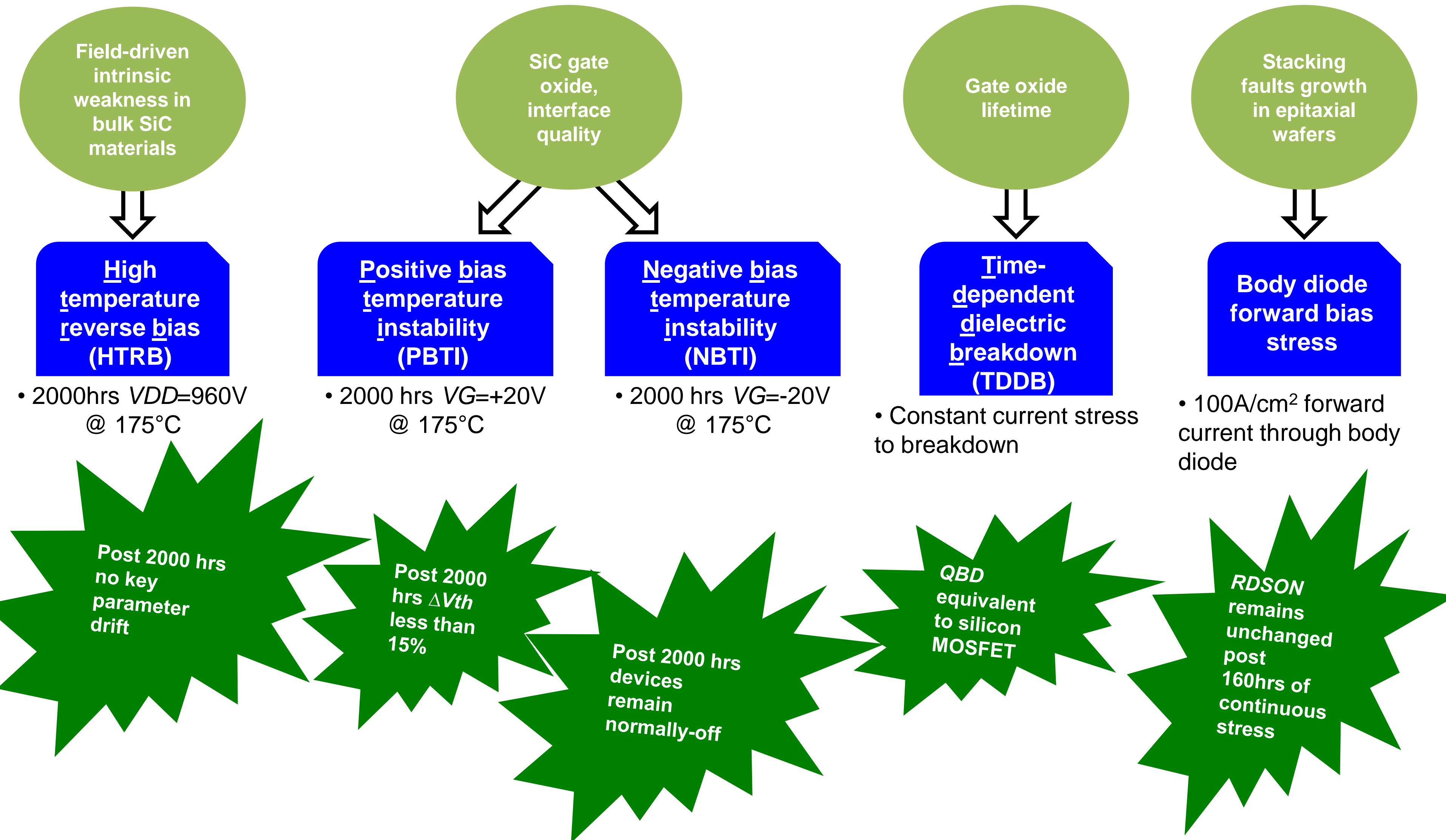
Reliable Technology Platform

SiC MOSFET Technology Reliability Assessment



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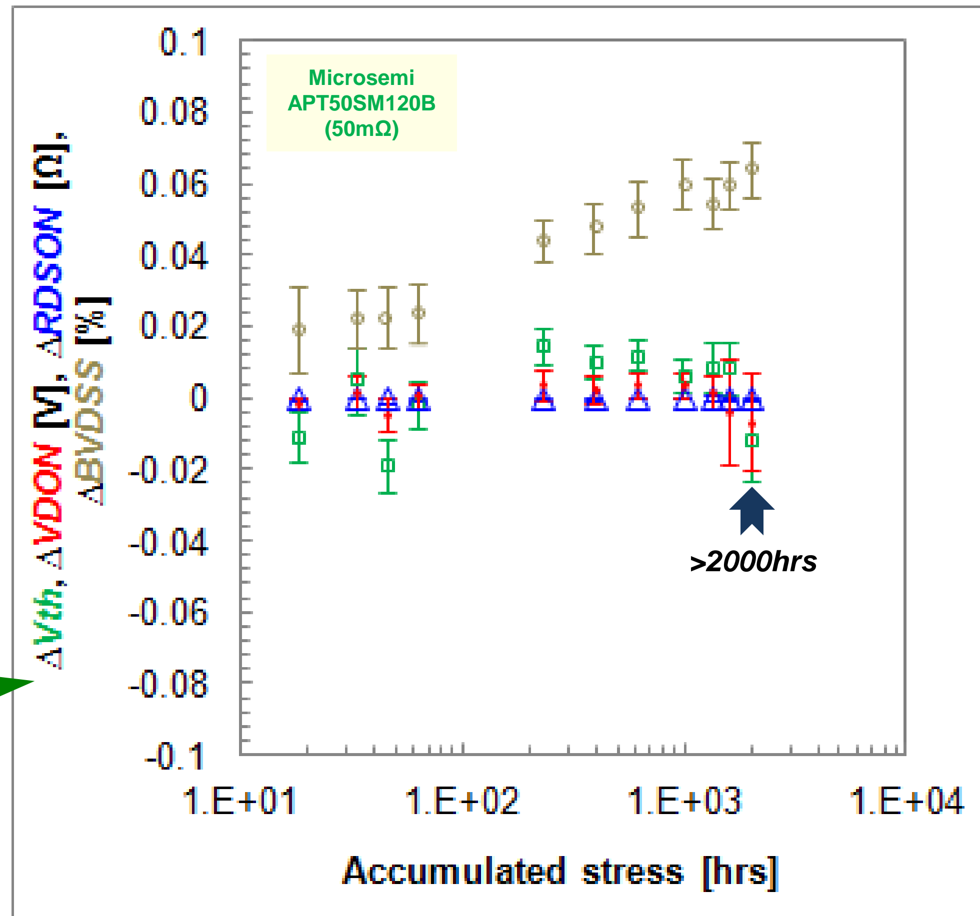
HTRB @ 175°C, 960V
(post 2000 hrs)

Field-driven intrinsic weakness in bulk SiC materials

High temperature reverse bias (HTRB)

- 2000hrs *VDD*=960V @ 175°C



Post 2000 hrs no key parameter drift

- No degrading drift of key electrical parameters post 2000 hrs

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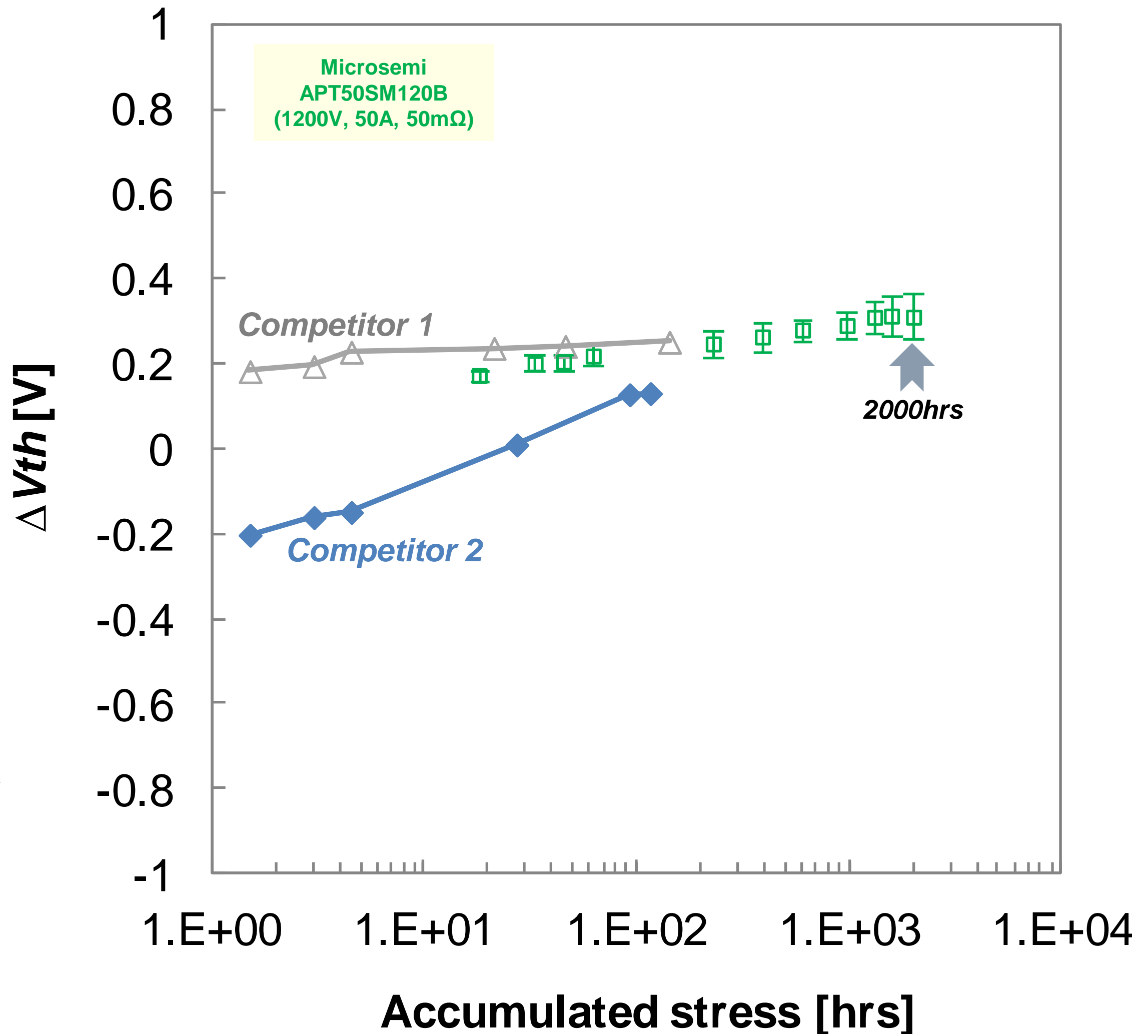
Gate Oxide Stability @ 175°C, *VG*=+20V
(PBTI post 2000hrs)

SiC gate oxide, interface quality

Positive bias temperature instability (PBTI)

- 2000 hrs *VG*=+20V @ 175°C

Post 2000 hrs Δ*Vth* less than 15%



- Device *Vth* drift less than 15% post 2000 hrs @ *VG*=+20V, 175°C (pre-stress *Vth*=2.7 ± 0.050V)

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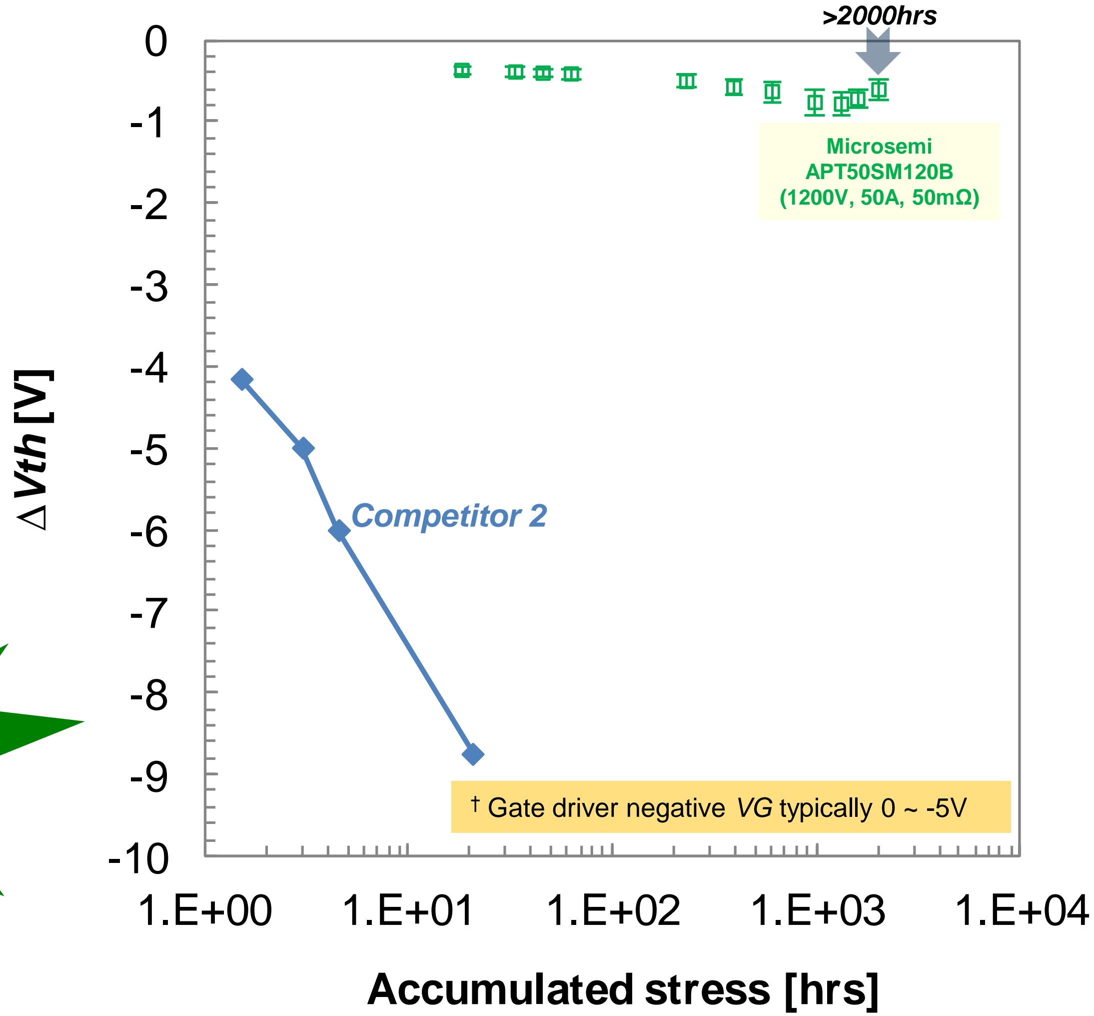
Gate Oxide Stability @ 175°C, *VG*=-20V
(NBTI post 2000hrs)

SiC gate oxide, interface quality

Negative bias temperature instability (NBTI)

- 2000 hrs *VG*=-20V @ 175°C

Post 2000 hrs devices remain normally-off



- Device remains normally-off post 2000 hrs @ *VG*=-20V, 175°C (pre-stress *Vth*=2.78 ± 0.070V)

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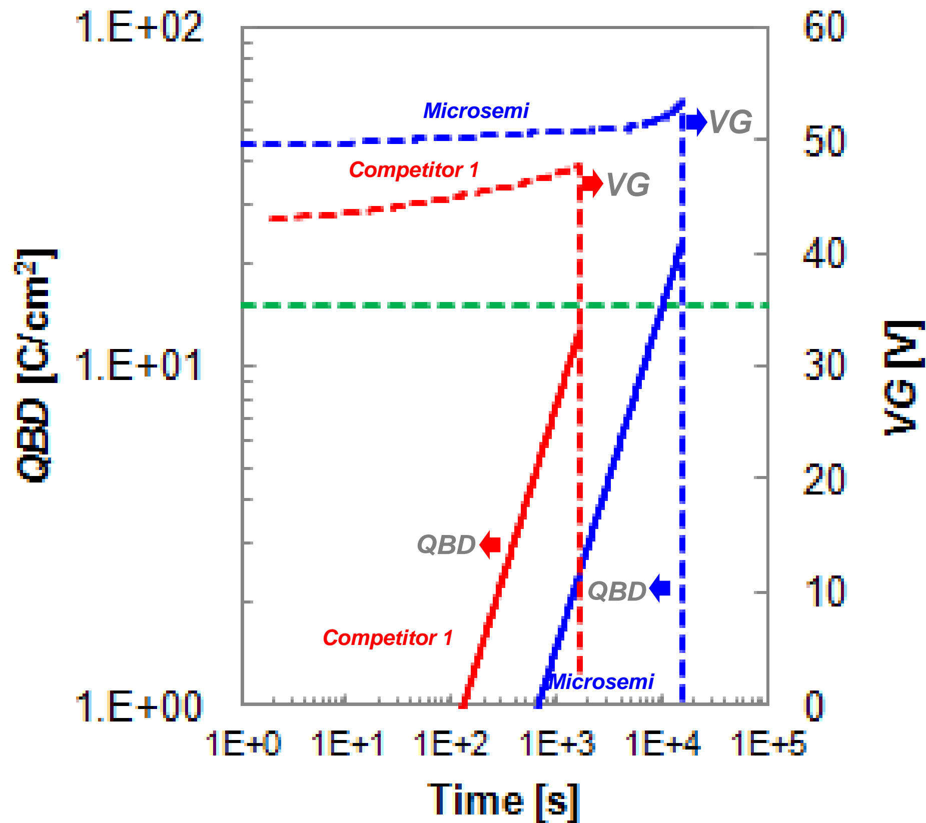
Time-Dependent Dielectric Breakdown (TDDB)

Time-dependent dielectric breakdown (TDDB)

- Constant current stress to breakdown

QBD equivalent to silicon MOSFET



- Constant current stress for all DUTs
- Si MOSFET *QBD* ~ 15-20C/cm^2 **(green dashed line)**

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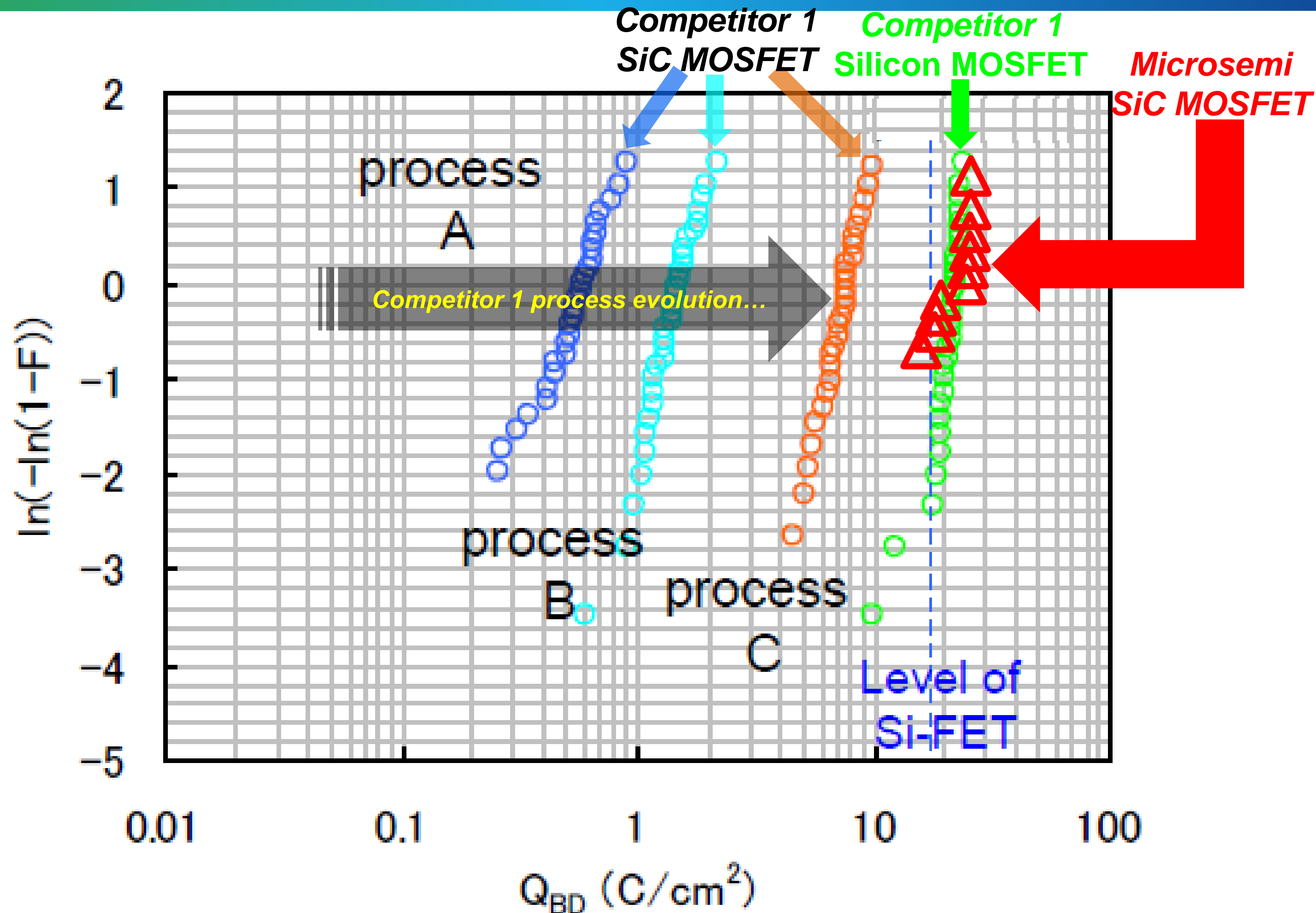
Gate Oxide Reliability Intrinsic Aging Lifetime Equivalent to Silicon ~300+ Years of Lifetime



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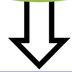
Body Diode Forward Stress

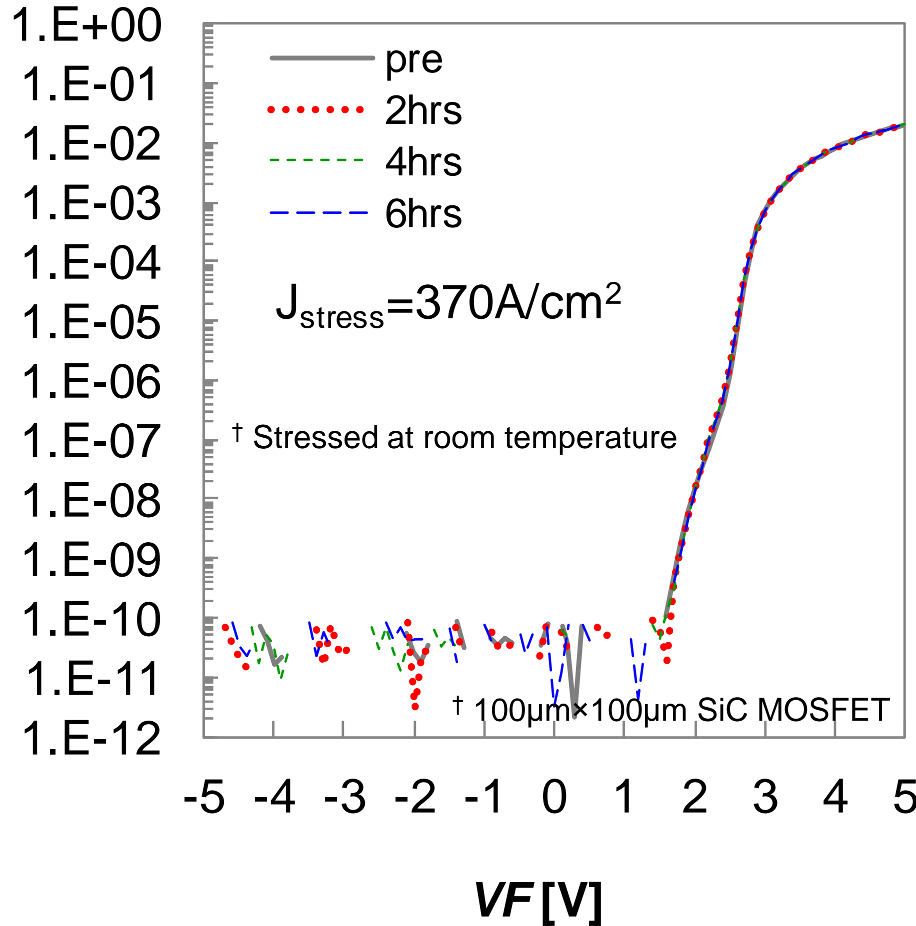
Stacking faults growth in epitaxial wafers



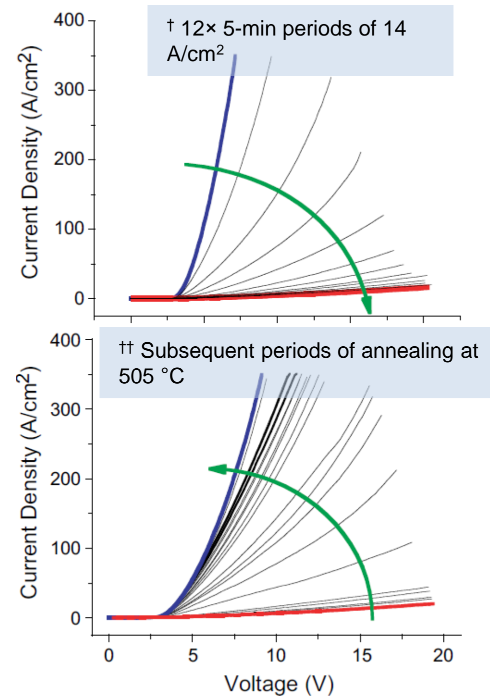
Body diode forward bias stress

- $100A/cm^2$ forward current through body diode

RDSON remains unchanged post 160hrs of continuous stress



Expansion of Shockley stacking faults (SSFs) during forward-bias device operation (stressing)



J.D. Caldwell et. al., 2008 NRL Review ELECTRONICS AND ELECTROMAGNETICS

- **High forward current density through body diode**
- **Body diode on-voltage, series resistance unchanged with stress time**

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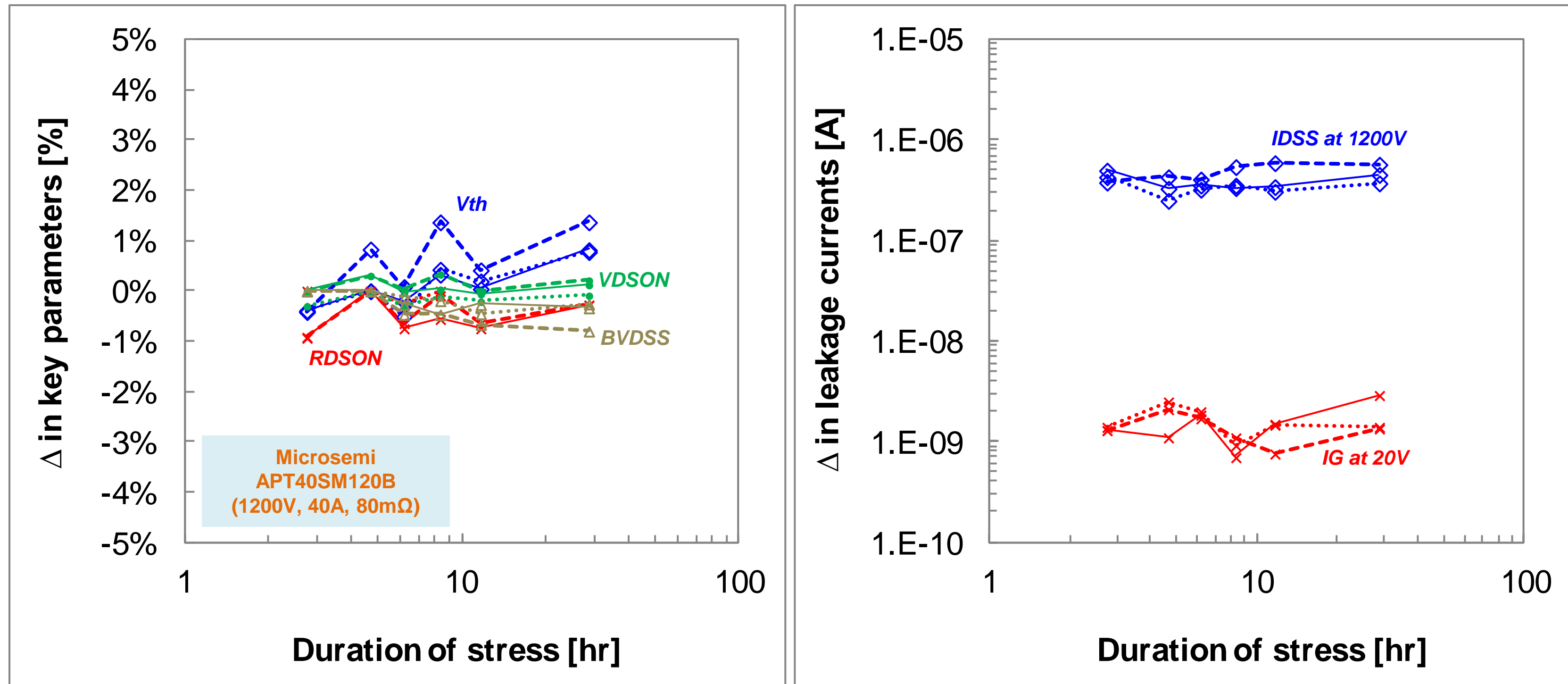
Medium-Current Body Diode Forward Stress 8A

† *G/S tied; 8A continuous forward current through body diode*



- **No evidence of Shockley stacking faults – high quality epitaxial wafers**

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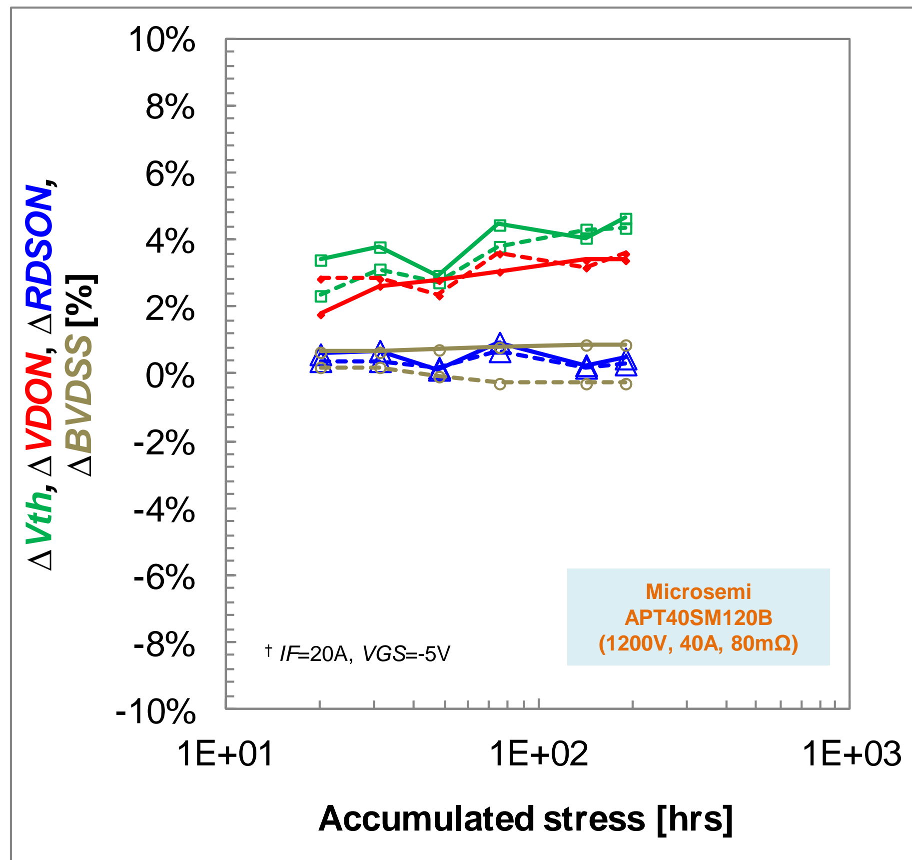
High-Current Body Diode Forward Stress 20A

† 20A continuous forward current through body diode



- **No evidence of Shockley stacking faults – high quality epitaxial wafers**

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Summary – Microsemi SiC MOSFETs

Microsemi's **Best-in-Class** SiC MOSFETs enable customers to design ultra efficient high power electronics

Microsemi Advantages

- Best-in-class $R_{DS(ON)}$ vs. Temperature
- Ultra Low Gate Resistance
- Low Conduction Losses
- Low Switching Losses
- Short Circuit Withstand Rated
- Reliable Technology Platform

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