# Highly Rugged 1200 V 80 mΩ 4-H SiC Power MOSFET

In-Hwan Ji, Amaury Gendron-Hansen, Mingyu Lee, Ed Maxwell, Bruce Odekirk, Dumitru Sdrulla, Changsoo Hong, Avinash S. Kashyap, and Faheem Faheem

Microsemi Corporation, 307 SW Columbia Street, Bend, OR 97702 USA

inhwan.ji@microsemi.com

***Abstract* — A novel 1200 V, 80 mΩ 4-H SiC power MOSFET with a shallow step p-body has been proposed for applications with highly rugged requirements. The innovative p-body design mitigates the problems arising due to the electric-field concentration at the corners that trigger the parasitic bipolar structure in conventional planar DMOS devices. TCAD simulations of the proposed device clearly demonstrate this improvement, along with significantly lower impact ionization rates at the corner of the p-body. The shallow step p-body approach, combined with a robust gate oxide and layout design, contributed to an industry-leading UIS capability of 2900 mJ of single pulse avalanche energy, and 5.8 µs of short circuit withstand time.**

***Keywords: 1200 V, SiC, Avalanche, Eas, UIS, Ruggedness, Power MOSFET, DMOS, Wide Bandgap***

## INTRODUCTION

The benefits of SiC power MOSFETs and their suitability for next-generation power electronics is well known [1-3]. For the widespread adoption of SiC products, the improvement of device robustness is essential to meet the end-user's needs in practical switching applications. In this paper, a new design concept of p-body implant for improving the avalanche capability is proposed. It is understood that the JFET region in the active cell is the electrically weakest area, when the device is under avalanche mode. The suppression of the induced hole current at the corner of the p-body is critical to improve avalanche capability [4-5]. The approach taken in this work is to mitigate the concentration of the electric field at the bottom of p-body by employing a shallow step p-body implant. To validate the proposed concept, we designed and fabricated 1200 V SiC power MOSFETs with the described enhancement. Un-clamped Inductive Switching (UIS) characterization was then carried out on multiple samples. The avalanche capability of the enhanced design was assessed by comparing the UIS results with the baseline deep p-body design.

## DEVICE STRUCTURES AND FABRICATION

The device structures of the proposed 4H-SiC power MOSFET with shallow step p-body (SSP) and conventional deep p-body (DP) are shown in Fig. 1. To design the junction depth of the SSP (Xj_2), 2D numerical simulations were performed using the Sentaurus TCAD tool [6]. The optimal Xj_2 over Xj_1 value was determined to be in the range of 0.6~0.7 based upon the assessment of the Baliga figure of merit [7]. This translates to the junction depth (Xj_1) of the conventional deep p-body to be around 30% deeper than that of the shallow step p-body (Xj_2). To fabricate the SSP, a split p-well implantation was implemented by applying 30% lower energy than the DP implantation.

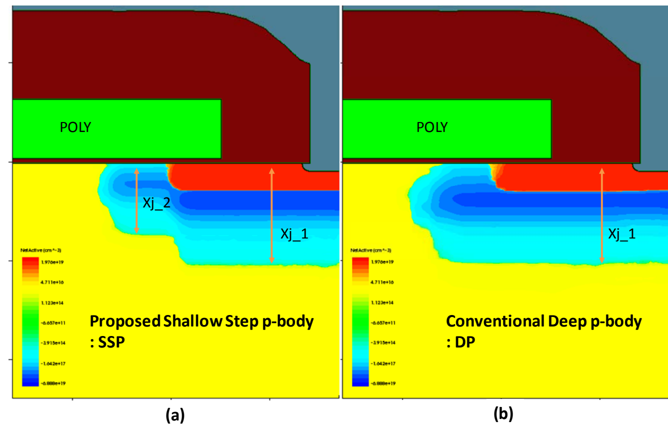


Fig. 1. Device structure of the proposed 4H-SiC Power MOSFET with (a) the shallow step p-body (SSP), and (b) conventional deep p-body (DP).

To achieve high channel mobilities and ensure reliable interface characteristics, the gate oxide was annealed in an NO ambient. Typical low field effect mobility was in the range of 17~20 $cm^2/(V \cdot s)$. A heavily doped poly-Si gate was introduced to achieve a low internal gate resistance (equivalent series resistance), thereby enabling high-speed switching applications. A TO-247 package build was utilized for the purpose of high current and high voltage characterization.

## SIMULATION AND EXPERIMENTAL RESULTS

TCAD simulations were performed to compare the output characteristics of the SSP and DP designs. Both devices demonstrate an $R_{ds,on}$ of 80 mΩ at a gate bias of 20 V at room temperature (Fig. 2). The simulated output characteristics were also validated with the measured data from the devices. For simulation accuracy, low field channel mobility has been calibrated empirically by employing the characterization of the interface trap density as outlined in [8]. The cross-sectional view of the fabricated SSP device is shown in Fig. 3 and it closely matches the TCAD structure presented in Fig. 1. In the SEM cross-section, the brighter area is the Al implanted zone.

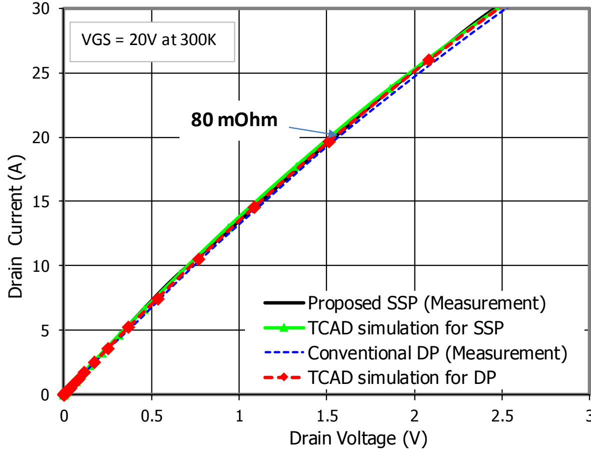


Fig. 2. Output characteristics of SSP and DP with $V_{GS}$ = 20 V at 300K.

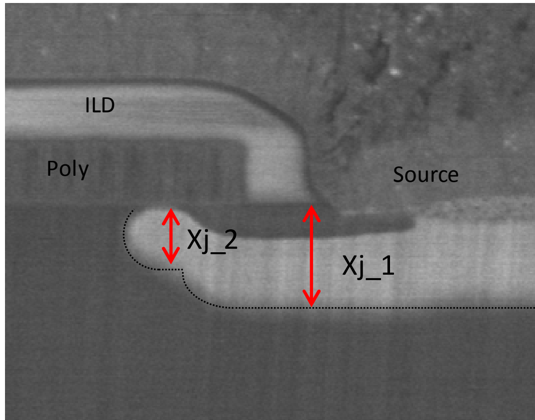


Fig. 3. SEM cross-sectional view of the fabricated SSP device.

To evaluate the avalanche capability, both devices have been tested employing a single pulse avalanche event with 20 A of $I_{ds}$ and a $V_{ds}$ of 50 V at room temperature. The results of the UIS test for SSP and DP devices are shown in Fig. 4. The new design achieved 2900 mJ of single pulse avalanche energy ($E_{as}$), while the DP device failed at an $E_{as}$ of just over 1100 mJ. This translates to a 2.6x higher avalanche capability for the new design.

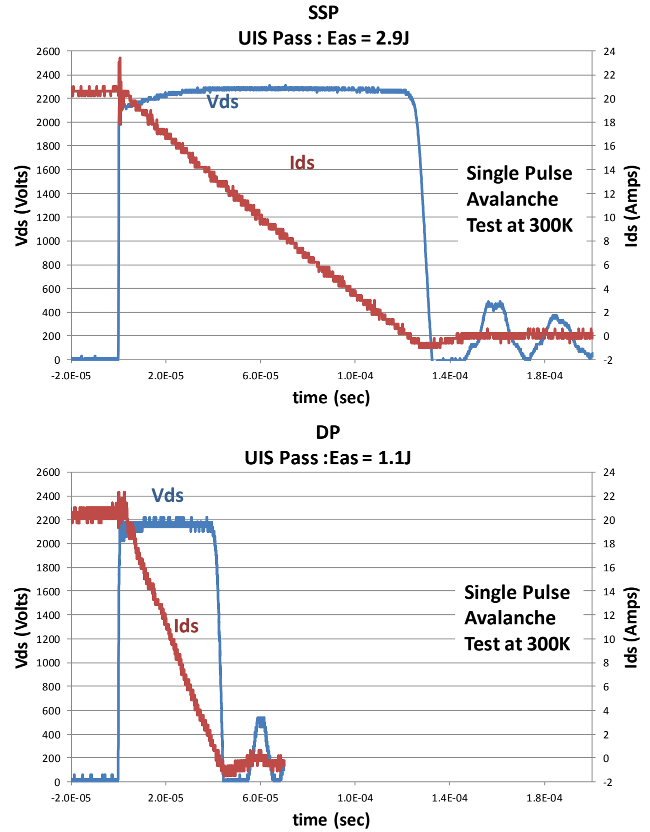


Fig. 4. UIS waveforms of SSP (above) and DP (below) designs.

It is common knowledge that the avalanche capability of power MOSFETs is strongly related to the suppression of the parasitic bipolar transistor [5]. To understand the underlying physics of the observed improvement in the SSP device, TCAD simulations under the UIS conditions were also performed. Thermal resistance values in the simulation were based on TO-247 packages. In order to shorten computation times, 200 mJ of $E_{as}$ were applied to both devices. As shown in Fig. 5a, at T=6 µsec, the electric field distribution (Fig. 5b) and the generation of the impact ionization (Fig. 5c) were extracted to evaluate the effectivity of the suppression of the parasitic bipolar transistor by the SSP structure. In Fig. 5b, the location of highest electric field of the SSP device has moved towards the source contact region due to the shallow step p-body, which results in decreasing the effective traveling distance of the hole current induced by avalanche breakdown. In addition, the magnitude of the peak electric field under the n+ source in the SSP structure has been mitigated by the e-field sharing with shallow p-body. The 1D profile of the electric field along the A-A’ cut (Fig. 5b) and impact ionization along the B-B’ cut (Fig. 5c) is shown in Fig. 5d. It should be noted that there is a 70% decrease of impact ionization in the SSP device as a result of the reduction in peak electric field shown in Figure 5b.

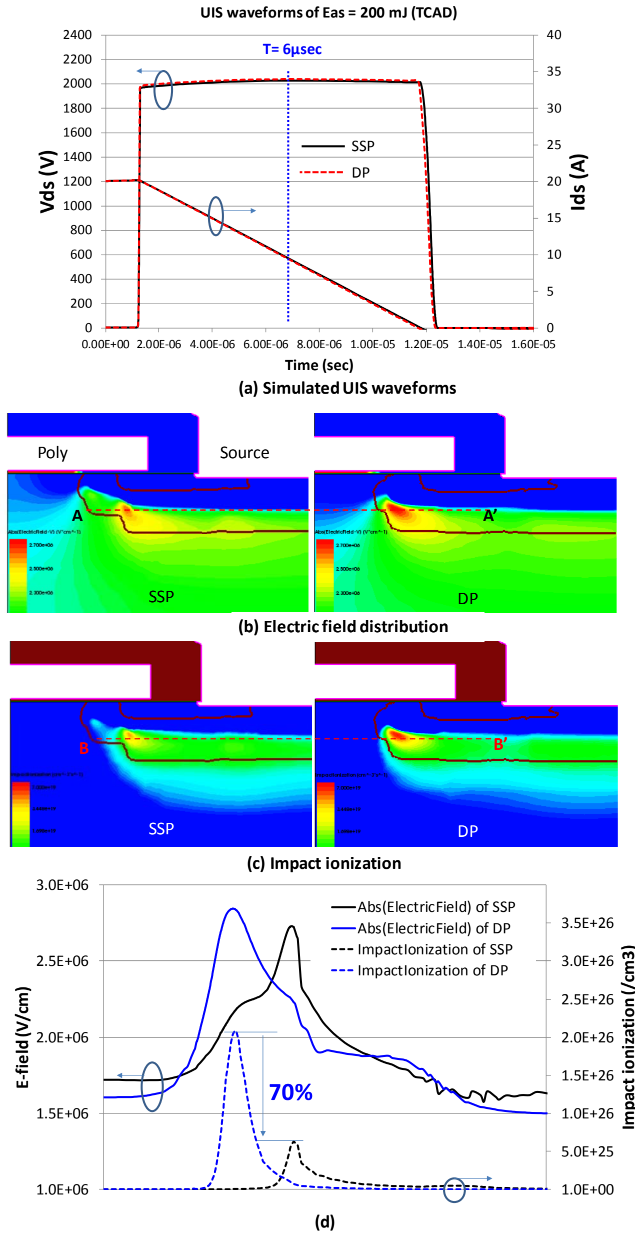


Fig. 5. (a) Transient simulation under UIS condition with 200 mJ of $E_{as}$ for SSP and DP, (b) 2D plots of the electric field distribution, (c) generation of impact ionization at 6 µsec and, (d) 1D profile of electric field along A-A' cut and impact ionization along B-B' cut.

Table 1 summarizes the electrical parameters of the SSP and DP MOSFETs. The threshold voltage ($V_t$) and $R_{ds,on}$ remain the same in both devices. The breakdown voltage (Fig. 6) of the SSP and DP at 1 mA of $I_{ds}$ is in the range of 1750~1850 V, which is within the tolerance of the epitaxy of commercial 4H-SiC wafers. When avalanche breakdown occurs in the device, the potential in the gate oxide also increases due to the presence of the JFET region. In the UIS simulations, the maximum electric field across the gate oxide reached up to 5 MV/cm. The integrity of the fabricated gate oxide is high enough to withstand the said avalanche stress. As shown in Fig. 7, the Fowler–Nordheim tunneling has been initiated at 7 MV/cm, demonstrating the robustness of the oxide.

Table 1. Summary of electrical parameters

| Device Structure | Xj_1 | Xj_2 /Xj_1 | $R_{ds,on}$ (mΩ) | $V_t$ (V) | $BV_{dss}$ (V) | $E_{as}$ at fail (J) |
|---|---|---|---|---|---|---|
| SSP | 1 | 0.6~0.7 | 80 | 2.7 | 1830 | 2.6~2.9 |
| DP | 1 | N/A | 80 | 2.7 | 1790 | 0.9~1.1 |

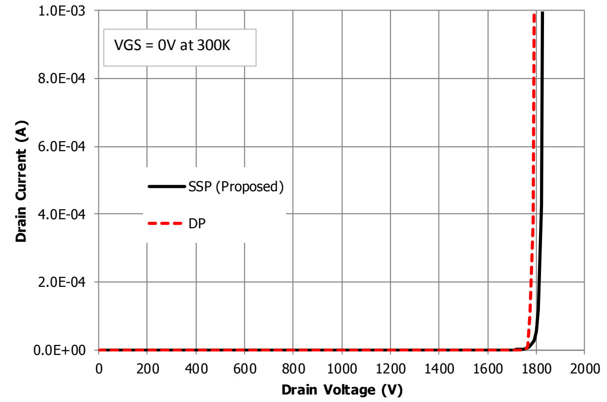


Fig. 6. Forward blocking characteristics of SSP and DP.

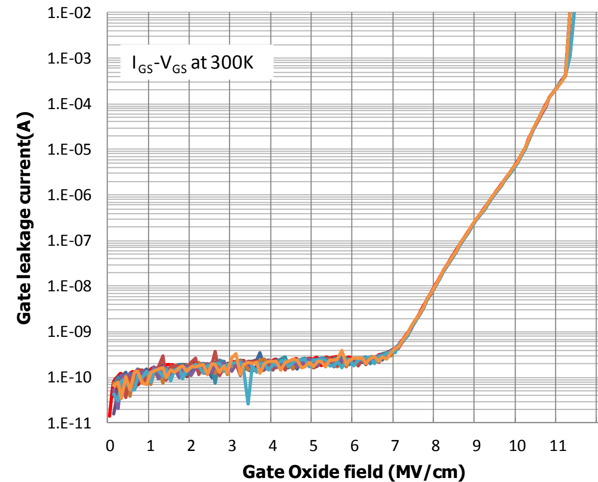


Fig. 7. Gate leakage current versus the electric field across the gate oxide.

The high quality gate dielectric prevents premature rupture during the avalanche condition, thereby improving the UIS capability. In order to verify the design robustness, standard post-failure analysis has been carried out on the SSP device that failed at 3000 mJ of $E_{as}$ (Fig. 8). A single burn mark induced by the destructive UIS test was observed in the decapped sample. It is assumed that the failure spot was generated randomly in the device active area, which is a desirable feature in terms of robustness. This is because it implies that the UIS capability is not limited by termination failure or corner effect.

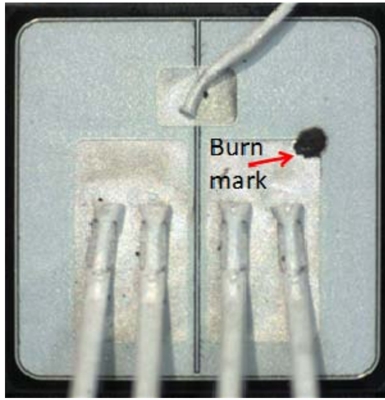


Fig. 8. Post-failure analysis of the proposed device failed at 3000 mJ of $E_{as}$.

It is widely accepted that the short-circuit withstand capability of 4H-SiC MOSFETs is not only limited by the peak saturation current ($I_{SC.peak}$), but also by the oxide robustness [9]. As shown in Fig. 9, the proposed SSP device exhibited excellent short-circuit withstand capability with a $T_{SC}$ of 5.8 µs at 960 V rail voltage. $I_{SC.peak}$ is in the range of 300 ~ 320 A. The total short-circuit withstanding energy ($E_{SC}$) of this device was 1200 mJ.

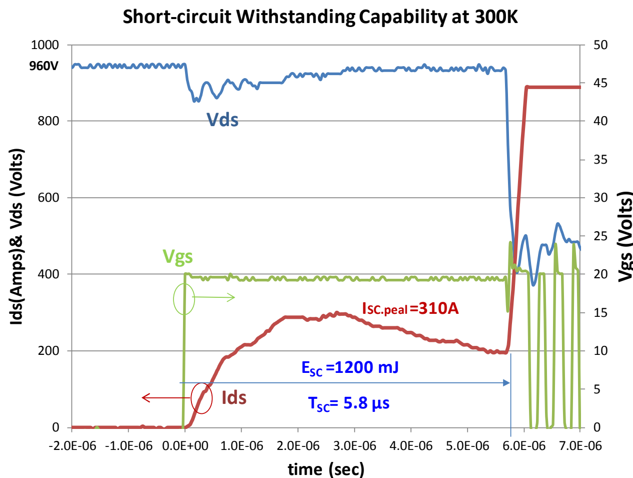


Fig. 9. Short-circuit withstand capability of the proposed SSP MOSFET (fault under load condition).

## SUMMARY

A new, highly rugged 1200 V 80 mΩ 4-H SiC power MOSFET with a shallow step p-body has been designed, fabricated, and validated by employing 2D numerical simulations and testing the avalanche capability. The novel shallow step p-body mitigates the concentration of the electric field at the corner of the p-body adjacent to the JFET region, resulting in suppression of the parasitic bipolar transistor and demonstration of and $E_{as}$ of 2900 mJ in a single pulse avalanche test. This device design is expected to increase the penetration of SiC devices in the automotive and industrial markets that require a high level of ruggedness.

## ACKNOWLEDGMENT

The authors would like to acknowledge the R&D support from the Microsemi Discrete Products Group. The contributions of the fabrication and characterization teams are also acknowledged, including those of Laird Thornhill, Terri Fields, Linda Starr, and William Brower.

## REFERENCES

[1] Palmour, J. W., L. Cheng, V. Pala, E. V. Brunt, D. J. Lichtenwalner, G-Y. Wang, J. Richmond et al. "Silicon carbide power MOSFETs: Breakthrough performance from 900 V up to 15 kV." In Power Semiconductor Devices & IC's (ISPSD), 2014 IEEE 26th International Symposium on, pp. 79-82. IEEE, 2014.

[2] Losee, P., A. Bolotnikov, L. Yu, R. Beaupre, Z. Stum, S. Kennerly, G. Dunne et al. "1.2 kV class SiC MOSFETs with improved performance over wide operating temperature." In Power Semiconductor Devices & IC's (ISPSD), 2014

[3] Banerjee, S., K. Matocha, K. Chatty, J. Nowak, B. Powell, D. Gutierrez, and C. Hundley. "Manufacturable and rugged 1.2 KV SiC MOSFETs fabricated in high-volume 150mm CMOS fab." In Power Semiconductor Devices and ICs (ISPSD), 2016 28th International Symposium on, pp. 279-282. IEEE, 2016.

[4] Ji, In-Hwan, Kyu-Heon Cho, Min-Koo Han, Sang-Chul Lee, Soo-Seong Kim, Kwang-Hoon Oh, and Chong-Man Yun. "New power MOSFET employing segmented trench body contact for improving the avalanche energy." In Power Semiconductor Devices and IC's, 2008. ISPSD'08. 20th International Symposium on, pp. 115-118. IEEE, 2008.

[5] Kim, Soo-Seong, Chong-Man Yun, Yearn-Ik Choi, and Min-Koo Han. "A new 600V PT-IGBT for the improved avalanche energy by employing the floating p-well." In Power Semiconductor Devices and ICs, 2003. Proceedings. ISPSD'03. 2003 IEEE 15th International Symposium on, pp. 71-74. IEEE, 2003.

[6] Synopsys, Sentaurus Device User Guide. Synopsys, 2016

[7] Baliga, B. J. "Semiconductors for high-voltage, vertical channel field-effect transistors." Journal of Applied Physics 53, no. 3 (1982): 1759-1764.

[8] Saks, N. S., S. S. Mani, and A. K. Agarwal. "Interface trap profile near the band edges at the 4H-SiC/SiO 2 interface." Applied Physics Letters 76, no. 16 (2000): 2250-2252.

[9] Nguyen, Thanh-That, Ashraf Ahmed, T. V. Thang, and Joung-Hu Park. "Gate oxide reliability issues of SiC MOSFETs under short-circuit operation." IEEE Transactions on Power Electronics 30, no. 5 (2015): 2445-2455.